

Energy-Efficient Architectures for Time-Critical LTE Protocol Stack Algorithms in Mobile Terminals

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The evolution of mobile communication systems aims at higher data rates in order to better support data-demanding mobile applications such as video streaming. The new Long Term Evolution (LTE) and LTE-Advanced (LTE-A) standards provide downlink transmission speeds of up to 300 Mbit/s and 3 Gbit/s, respectively. To cope with such high data rates, the processing of the modem protocol stack must be performed within tight timing constraints. Furthermore, protocol processing must be implemented to consume a minimal amount of energy in order to enable a longer battery lifetime. Additionally, as more and more features are being integrated in mobile handsets, area-optimized designs are also required to reduce chip costs. Due to these design challenges, new architectural solutions targeting the challenging protocol processing speed requirements are investigated and explored in this thesis.

This work addresses the time-critical algorithms in the modem protocol stack, i.e. the ciphering required for data protection and the Robust Header Compression (ROHC) scheme employed to improve the utilization of radio link bandwidths. In particular, software and hardware architectures for the time-critical algorithms are proposed, targeting an optimization of processing speed and energy consumption.

The proposed software architectures focus on embedded multi-core processing for parallel execution of ciphering algorithms. For profiling and analysis of software implementations, a multi-core based virtual prototype and an event-based energy model are developed. The SNOW 3G cipher is efficiently partitioned for parallel processing on two cores and its cryptographic substitution boxes (S-Boxes) are optimized by minimizing their demand for memory resources. Moreover, the Advanced Encryption Standard (AES) is implemented to exploit the processor's architectural width via sliced multi-block encryption, wherefore it is parallelized on four cores to encrypt/decrypt four data blocks simultaneously. The proposed software optimizations achieve a maximum processing throughput of 300 Mbit/s. For the first LTE category (100 Mbit/s), voltage and frequency scaling is applied to exploit extra performance delivered by parallelism, where energy savings of 70% are obtained compared to non-optimized single core implementations.

Since software processing capabilities are limited to LTE speeds, hardware acceleration for ciphering and header compression is considered in the second part of this thesis. Consequently, the hardware designs proposed in this work aim at processing speeds that are high enough for LTE-A data rates and beyond with the focus on energy and area minimization. First, ZUC and SNOW 3G ciphers are analyzed. The shift register and the S-Boxes are identified as the most power demanding functions. A unified hardware accelerator combining both ciphers is presented, in which the S-Boxes are merged based on one-hot encoding and the shift register is split into parallel segments. Hardware designs are modeled in VHDL and synthesized using 90 nm standard cell ASIC technology. The integrated hardware accelerator supports data rates of up to 10 Gbit/s. Compared to conventional stand-alone hardware accelerators, area and power consumption are simultaneously reduced by 35% and 40%, respectively. In addition, a parallel architecture for the Least Significant Bit (LSB) encoding scheme in ROHC is developed based on unary and one-hot bit encodings. This results in an area reduction of 36% and energy savings of 50% compared to the existing loop-based implementation.

The software and hardware architectures presented in this work provide a solution for high-performance and energy-efficient baseband processing in future LTE mobile handsets. This work is distinguished as the first one to provide an optimized parallel partitioning of SNOW 3G for embedded multi-core processing and novel light-weight hardware architecture for LSB encoding, which is responsible for header compression.